IN THE CLAIMS

1 (Previously Presented). A semiconductor package, comprising:

a substrate having a resin layer with first and second surfaces wherein a plurality of electrically conductive patterns are formed thereon, the resin layer having an aperture formed in a central area thereof;

a solder mask formed on the first and second surfaces of the substrate, the solder mask covering the electrically conductive patterns;

a first semiconductor chip having first and second surfaces, the second surface having a plurality of input/output pads formed thereon, the first semiconductor chip being placed in the aperture of the substrate;

a plurality of first conductive wires for connecting the input/output pads of the first semiconductor chip to the electrically conductive patterns formed on the resin layer;

an adhesive attached to the second surface of the first semiconductor chip;

a second semiconductor chip having first and second surfaces, the second surface having a plurality of input/output pads formed thereon, the second semiconductor chip being attached to the adhesive;

a plurality of second conductive wires for connecting the input/output pads of the second semiconductor chip to the electrically conductive patterns formed on the resin layer;

an encapsulate for encapsulating the aperture, the first and second semiconductor chips, and the first and second conductive wires; and

a conductive thin film extending across the aperture of the substrate and coupled to the first side of the first semiconductor chip and the solder mask formed on the first surface of the substrate, the conductive thin film electrically coupled to the electrically conductive patterns formed on the first surface of the substrate through openings formed in the solder mask.

2 (Previously Presented). The semiconductor package in accordance with Claim 1 wherein each of first conductive wires are stand off stitch bonded.

3 (Previously Presented). The semiconductor package in accordance with Claim 1 wherein one end of each first conductive wire is ball-bonded to one of the electrically conductive patterns and the other end is stitch-bonded to one of the input/output pads of the first semiconductor chip.

4 (Original). The semiconductor package in accordance with Claim 3 wherein a conductive ball is coupled to the input/output pad of the first semiconductor chip and the first conductive wire is stitch-bonded to the conductive ball.

5 (Previously Presented). The semiconductor package in accordance with Claim 3 wherein each of the plurality of second conductive wires for connecting the input/output pads of the second semiconductor chip to the electrically conductive patterns on the resin layer of the substrate are normal wire bonded.

6 (Previously Presented). The semiconductor package in accordance with Claim 3 wherein one end of each second conductive wire is ball-bonded to one of the electrically conductive patterns and the other end is stitch-bonded to one of the input/output pads of the second semiconductor chip.

7 (Original). The semiconductor package in accordance with Claim 6 wherein a conductive ball is fused to the input/output pad of the second semiconductor chip and the second conductive wire is stitch-bonded to the conductive ball.

8 (Previously Presented). The semiconductor package in accordance with Claim 1 wherein the conductive thin film absorbs electromagnetic waves.

9 (Previously Presented). The semiconductor package in accordance with Claim 8 wherein the electrically conductive patterns are formed on the first and second surfaces of the resin layer and are connected through at least one conductive via.

10 (Original). The semiconductor package in accordance with Claim 9 wherein the electrically conductive patterns formed on the second surface of the resin layer are electrically connected to the conductive thin film.

11 (Previously Presented). The semiconductor package in accordance with Claim 1 wherein the adhesive is silicon having an adhesive layer formed on a top and bottom surface thereon.

12 (Original). The semiconductor package in accordance with Claim 1 wherein the second semiconductor chip has an insulating layer formed on the first surface thereof.

13 (Original). The semiconductor package in accordance with Claim 1 wherein the horizontal width of the second semiconductor chip is wider than that of the first semiconductor chip.

14 (Previously Presented). A semiconductor package, comprising:

a substrate having a resin layer with first and second surfaces wherein a plurality of electrically conductive patterns are formed thereon, the resin layer having an aperture formed at a central area thereof;

a solder mask formed on the first and second surfaces of the substrate, the solder mask covering the plurality of electrically conductive patterns;

a first semiconductor chip having first and second surfaces, the second surface having a plurality of input/output pads formed thereon, the first semiconductor chip being placed in the aperture of the substrate;

a plurality of first conductive wires for connecting the input/output pads of the first semiconductor chip to the electrically conductive patterns formed on the resin layer;

a second semiconductor chip having first and second surfaces, the second surface having a plurality of input/output pads formed thereon;

means coupled to the second surface of the first semiconductor chip for coupling the first semiconductor chip to the second semiconductor chip;

a plurality of second conductive wires for connecting the input/output pads of the second semiconductor chip to the electrically conductive patterns formed on the resin layer;

means for encapsulating the aperture of the substrate, the first and second semiconductor chips, and the first and second conductive wires; and

a conductive thin film extending across the aperture of the substrate and coupled to the solder mask formed on the first surface of the substrate, the conductive thin film electrically coupled to the electrically conductive patterns formed on the first surface of the substrate through openings formed in the solder mask.

15 (Previously Presented). The semiconductor package in accordance with Claim 14 wherein one end of each first conductive wire is ball-bonded to one of the electrically conductive patterns and the other end is stitch-bonded to one of the input/output pads of the first semiconductor chip so that a curved portion of the first conductive wire is placed on the electrically conductive pattern.

16 (Previously Presented). The semiconductor package in accordance with Claim 14 wherein one end of each second conductive wire is ball-bonded to one of the electrically conductive patterns and the other end is stitch-bonded to one of the input/output pads of the second semiconductor chip so that a curved portion of the second conductive wire is placed on the electrically conductive pattern.

17 (Previously Presented). The semiconductor package in accordance with Claim 14 wherein the conductive thin film absorbs electromagnetic waves and dissipates heat from the first semiconductor device.

18 (Original). The semiconductor package in accordance with Claim 17 wherein the electrically conductive patterns formed on the second surface of the resin layer are electrically connected to the conductive thin film.

19 (Original). The semiconductor package in accordance with Claim 14 wherein the second semiconductor chip has an insulating layer formed on the first surface thereof.

20 (Previously Cancelled).

21 (Previously Cancelled).

22 (Previously Cancelled).

23 (Previously Cancelled).

24 (Previously Cancelled).

25 (Previously Cancelled).

26 (Previously Cancelled).

27 (Previously Presented). A semiconductor package, comprising:

a substrate having a resin layer with first and second surfaces wherein a plurality of electrically conductive patterns are formed thereon, the resin layer having an aperture formed in a central area thereof;

a solder mask formed on the first and second surfaces of the substrate, the solder mask covering the electrically conductive patterns;

a thin conductive film placed over the aperture and coupled to the solder mask on the first surface of the substrate, the conductive film coupled to the electrically conductive patterns on the first surface of the resin layer through openings formed in the solder mask;

a first semiconductor chip having a first surface coupled to the thin conductive film and a second surfaces having a plurality of input/output pads formed thereon;

a second semiconductor chip having a first surface coupled to the first semiconductor chip and a second surface having a plurality of input/output pads formed thereon;

an encapsulate for encapsulating the aperture and the first and second semiconductor chips.

28 (Previously Presented). A semiconductor package in accordance with Claim 27 further comprising a plurality of first conductive wires for connecting the input/output pads of the first semiconductor chip to the electrically conductive patterns formed on the second surface of the resin layer.

29 (Previously Presented). A semiconductor package in accordance with Claim 27 further comprising a plurality of second conductive wires for connecting the input/output pads of the second semiconductor chip to the electrically conductive patterns formed on the second surface of the resin layer.

30 (Previously Presented). A semiconductor package in accordance with Claim 27 further comprising an adhesive attached to the second surface of the first semiconductor chip.

31 (Previously Presented). A semiconductor package in accordance with Claim 27 further comprising a plurality of conductive balls coupled to the electrically conductive patterns formed on the second surface of the resin layer.